

EEEC382

Experiment Introduction to Altera Quartus II Software

1 Purpose

Perform basic schematic capture and simulation with Altera Quartus software.

2 Prelab

- Browse the tutorial article, *Quartus II Introduction Using Schematic Design*. The download link can be found on the class web page http://academic.csuohio.edu/chu_p/EEEC382.html
- Drive the logic expressions and truth table in 3.9(a)(b)(c)

3 Procedures

Altera provides a good tutorial article, titled *Quartus II Introduction Using Schematic Design*. However, this tutorial is intended for implementing the circuit with FPGA devices. We only use it for schematic and simulation for now. The following procedure modifies the tutorial for this purpose. The Quartus II web edition can be freely downloaded and installed in your home PC. The link can be found in the class web page.

3.1 Logon in SH309

A user account is needed to access a PC in SH309.

(a) Logon

- The user name is your first letter of first name plus last name. For example, John Doe's user name will be "jdoe".
- The initial password is "password".
- Logon procedure:
 - Press Control, Alt and Delete keys at the same time.
 - Make sure you log onto DIGITLLAB domain.
 - Type your user name and initial password. You will be prompted to change your password.

(b) Altera license setup

For PCs in SH309, Altera Quartus II requires accessing a license file to operate. If it is not done automatically, manually set up the file as follows:

- Select Tools menu and then License Setup... A dialog window pops up.
- Type 1717@ecesvr in the License File field. Close the window

3.2 Create a project (section 2 of tutorial)

A Quartus project specifies the working directory, device, and various design files. Follow the tutorial but with the following modification:

- (a) In step 2, create the working directory in the network drive (H:\your_name) or thumb drive.

(b) In step 4, select the chip as follows:

family: Cyclone II, device: EP2C20F484C7

If you are not sure, just check the marking on the chip. The device assignment can be changed later via Assignments menu.

3.3 Enter the schematic using the graphic editor (section 3)

Follow the tutorial.

3.4 Compiling (section 4)

- (a) Follow the tutorial to “compile” the design. Altera invents its own term for various processes. The term *compile* is the overall process that consists of four smaller processes: *Synthesis* (the usual), *Fitter* (placement/routing), *Assembler* (generating configuration file) and *Timing analyzer*.
- (b) A detailed report is generated after compiling. Several info items are of interest to us:
- Area (size of the circuit, in terms of number of LEs): in Compilation Report Window, select Fitter > Summary and look at Total logic elements.
 - Performance (in terms of worst propagation delay): in Compilation Report Window, select Timing Analyzer > Summary and look at Worst-case tpd
 - Pin assignment: in Compilation Report Window, select Fitter > Pin-out file or Fitter > Resource Section > Input/Output Pins.

3.5 Pin assignment (section 5)

Pin assignment is the process of assigning physical pins to the I/O signals. If unspecified, Quartus automatically selects the physical pins. In DE1 board, I/O pins of the FPGA device are permanently connected to I/O peripherals on the printed circuit board, we must force the pin assignment during the process. The permanent pin connections of DE1 board can be found in the DE1 manual.

- (a) Follow the tutorial, but assign x1, x2 to two switches of EP2C20 (pin L22 and pin L21) and f to an LED (pin R20).
- (b) Recompile the design with the pin assignment.
- (c) Check the report to ensure that the pin assignment actually takes effect.

3.6 Simulation (section 6)

To perform simulation, we first create the test vectors (input patterns) in waveform editor and save the file, and then simulate the circuit operation with these test vectors.

- (a) Follow step 1 to create a light.vwf file (test vector waveform).
- (b) In step 2, set the time grid to 100 ns by selecting Edit > Grid Size and set the simulation interval to 1 μ s by selecting Edit > End time. The 100 ns-grid makes the propagation delay portion smaller and easier to check the response.
- (c) Follow steps 3 and 4, but use 100 ns grid instead.
- (d) Skip 6.1.1 and continue to 6.1.2 to perform timing simulation. Note that the simulated output waveform is in Simulated Report – Simulation Waveforms window rather than the light.vwf file.
- (e) Print the schematic and simulation diagram.

3.7 Device programming (section 7)

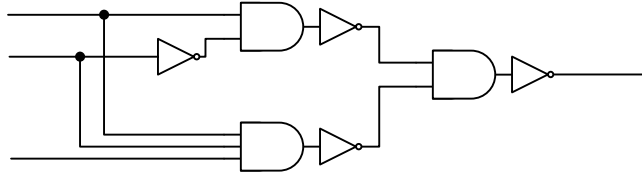
Follow the instruction in section 7.1 to program the FPGA chip.

3.8 Testing the physical circuit

Test the circuit with the two switches on DE1 board and observe the LED. ©

3.9 Combinational circuit analysis

Consider the following circuit



- Derive the logic expression for the circuit.
- Convert the expression to SOP format
- Derive the truth table for the circuit
- Follow the previous tutorial to perform schematic entry and simulation.
- Print the schematic and simulation diagram
- Compare the simulation result with the truth table and verify the circuit operation.
- Perform pin assignment (note that there is one new input pin. The assignment can be found on course web page.
- Program the device and test the physical implementation. Compare the result with truth table. ©

a

b

c

Signature Sheet

Section 3.8: _____.

Section 3.9(h): _____.