

## Chapter 11: Digital Data Acquisition

Topics:

Binary Representation

Quantization and Resolution

A/D and D/A Conversion

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## Binary Data Representation

Digital equipment store quantities using only two available digits: 0 and 1, which correspond to off and on states of transistors.

Only a finite number of digits (bits) are available to represent quantities.

For instance, with 3 bits, we can only represent

000,001,010,011,100,101,110,111. That is, only  $2^3=8$  numbers.

This implies that any correspondence between the above binary numbers and “real world” numbers will be imperfect.

There are two fundamental limitations: *range* and *resolution*.

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# Range and Resolution

Range, also called Full Scale, or FS, is the range of the analog quantity to be digitized. If we use 3 bits to capture a 5-10 V range, then  $FS = 5$ .

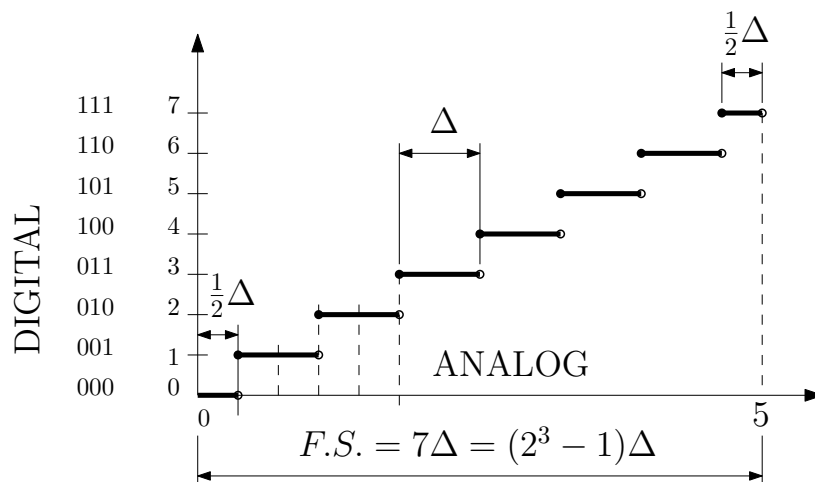
Resolution is a measure of the granularity of the data. If we have 3 bits, then we have 8 representable numbers. We have only 7 slots to accommodate any analog quantity in the 0-5 range.

This means that any voltage between 0 and  $5/14$  will be called 000, any voltage between  $5/14$  and  $15/14$  will be 001, and so forth, until we hit the  $[65/14, 5]$  range, which we associate with 111.

If the number of bits is  $k$ , the resolution is  $\frac{FS}{(2^k - 1)}$ .

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## Ideal 3-bit Conversion Mapping



The *quantization uncertainty* is half the resolution.

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# Binary, Hexadecimal and Decimal Conversions

- Decomposition of a base-10 number:

$$153 = 1 \times 10^2 + 5 \times 10^1 + 3 \times 10^0$$

- Decomposition of a base-2

$$\text{number: } 10111_2 = 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 = 23$$

- The leftmost digit is called the *most significant bit* (MSB), while the rightmost digit is the *least significant bit* (LSB).
- Convert a decimal number to binary by successive division by 2. The result is the sequence of remainders in reverse order (the MSB is the last remainder).
- Example: Convert 23 back to base 2.
- Integer binary arithmetic is similar to decimal case. Check by performing a few  $+$ ,  $-$ ,  $\times$ ,  $\div$

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## More on Binary Arithmetic

- Divide binary integers by repeated subtraction of divisor. Set quotient to zero. Add 1 to the quotient after each subtraction. Repeat until subtraction is smaller than divisor. This is the remainder. Example:  $1001_2 \div 10_2$ .
- Fractional binary numbers:  
$$0.1101_2 = 0 \times 2^0 + 1 \times 2^{-1} + 1 \times 2^{-2} + 0 \times 2^{-3} + 1 \times 2^{-4}$$
- Convert decimal fraction to binary by successive multiplication by 2: separate integer and fractional parts. Integer parts are the binary digits. Continue until fractional part is zero.
- Example: convert 0.125 to binary.
- Note: Non-periodic decimal fractions can result in periodic binary fractions. (Convert 0.4)

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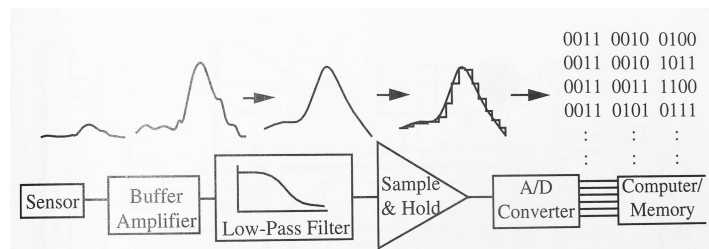
# More on Binary Arithmetic

- Binary is as easy as 1, 10, 11
- There are 10 kinds of people in the world - those who understand binary numbers, and those who don't.
- Hexadecimal numbers:  
0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F.
- To go from binary to hex, group in fours and translate directly:  $1111011_2 = 7B_{16}$
- Exercise: How many people can read hex if only you and DEAD people can read hex?

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## Digital Data Acquisition System



- The buffer, if required, presents a large input impedance to the sensor and amplifies its output.
- The filter reduces the bandwidth of the incoming signal to reduce the noise and avoid aliasing errors.
- The sample-and-hold maintains the signal constant so that the conversion is performed accurately.
- The DAC digitizes the signal.

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# Analog-to-Digital Conversion Principles

In ADC we take a sample of an analog voltage and represent it using the available number of bits.

ADC converters usually require a *sample-and-hold* (S&H) circuit at their input. The S&H captures the voltage and holds it constant for the converter to carry its operation.

The ADC uses two constant reference voltages. If the voltages are positive and negative ( $\pm 10\text{V}$ ), the ADC is *bipolar*. If the voltages are zero and another value, the ADC is *unipolar*. The input signal is expected to fall within the range of the reference voltages.

The ADC will assign the maximum representable binary to an input voltage equal to the positive reference. If so configured, it will assign 0 to an analog input voltage equal to the lower reference voltage. ADC's can also be programmed to reserve one bit for sign.

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## Examples

A unipolar, 12-bit ADC uses a reference voltage of +5V. Find the binary representation of an analog input voltage of 3.56 V. Assume that the coding is such that 0V corresponds to 000000000000.

A bipolar, 10-bit ADC uses reference voltages of  $\pm 10\text{V}$ . Find the binary representation of an analog input voltage of -3.56V. Assume that the coding is such that the MSB is used for sign (1 means negative). Observe the issue of having two representations for zero.

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# Successive Approximation ADC Technique

This method begins by initializing all bits to 0 and then setting the MSB to 1 as a first estimate.

This estimate is converted to an analog voltage (DAC) and compared to the analog voltage  $v_i$  being converted. If  $v_i$  was exceeded, the MSB is cleared.

Then the next bit is set and the process is repeated until the LSB is reached.

As you can tell, this method requires DAC hardware and it relies on a constant analog input voltage. Errors can occur for fast-changing voltages.

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## Dual-Slope ADC Technique

The *dual-slope* conversion technique relies on an integrating circuit process (capacitor charge).

The analog voltage  $V_i$  is applied as the input to an integrating circuit.

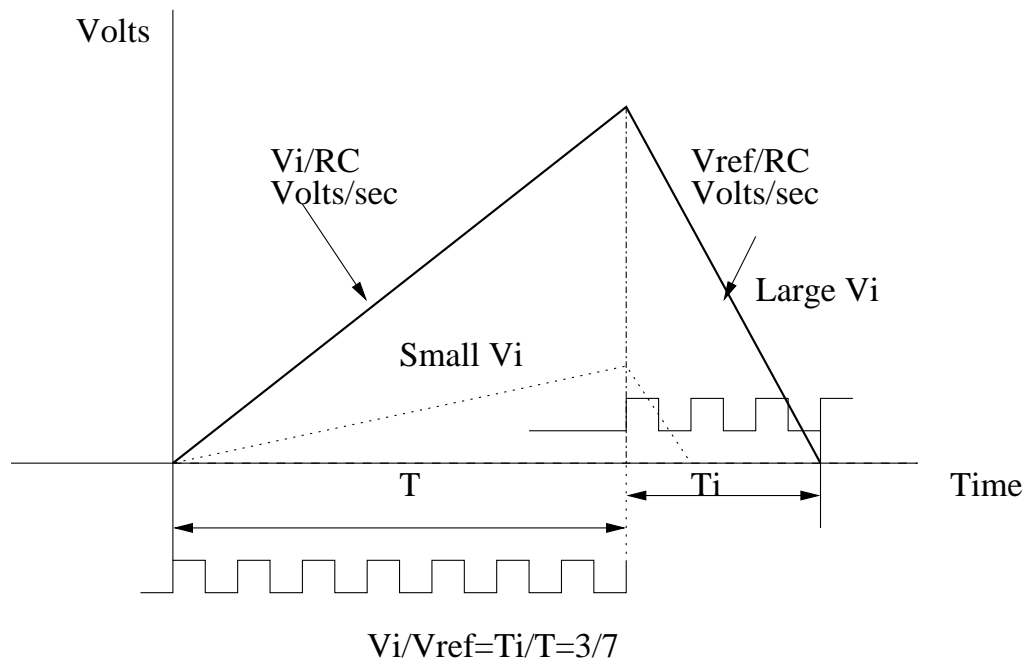
The integration is continued for a fixed period of time,  $T$ .

The input to the integration is switched to the negative reference voltage  $V_R$  and a time counter is started.

When the output of the integrator reaches 0 again, the counter is stopped, giving a value  $T_i$ .

Since the ratio of the ramp-up and ramp-down times equals  $V_R/V_i$ , the voltage can be digitized.

# Dual-Slope ADC

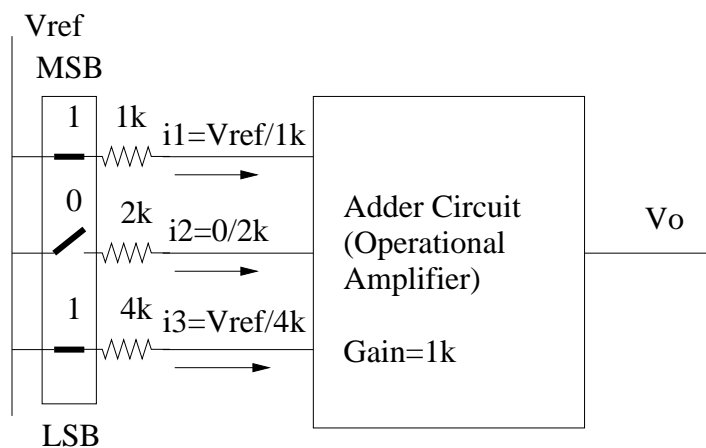


Disadvantage: slow process. Advantage: Independent of component inaccuracy (R,C).

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## Digital-to-Analog Conversion Principles

Most DAC methods involve the decomposition of a binary number, for example  $10111_2 = 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 = 23$ . The analog voltage is a weighted sum of bits (0 or 1), where the weights are 1, 2, 4, 8, etc. If we use resistors as weights and a special adder circuit, we can obtain the required voltage:



$$V_o = 1k * V_{ref} * (1/1k + 0/2k + 1/4k) = 1.25V_{ref}$$

$V_o$  ranges from 0 to 7 $V_{ref}$

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# R-2R DAC

The weighted DAC requires unreasonable resistor values. For a 12-bit DAC, if the MSB is 1k, the LSB must be  $2^{11} = 2048k$ , or  $2.048M\Omega$ , which is difficult to obtain with accuracy. We need 12 precision resistors.

The R-2R DAC solves this problem:

