

# Homework #1 (Due Tue, Sep. 11)

## EEC 581, Fall 2007

1. Exercise 1.7
2. Exercise 1.14

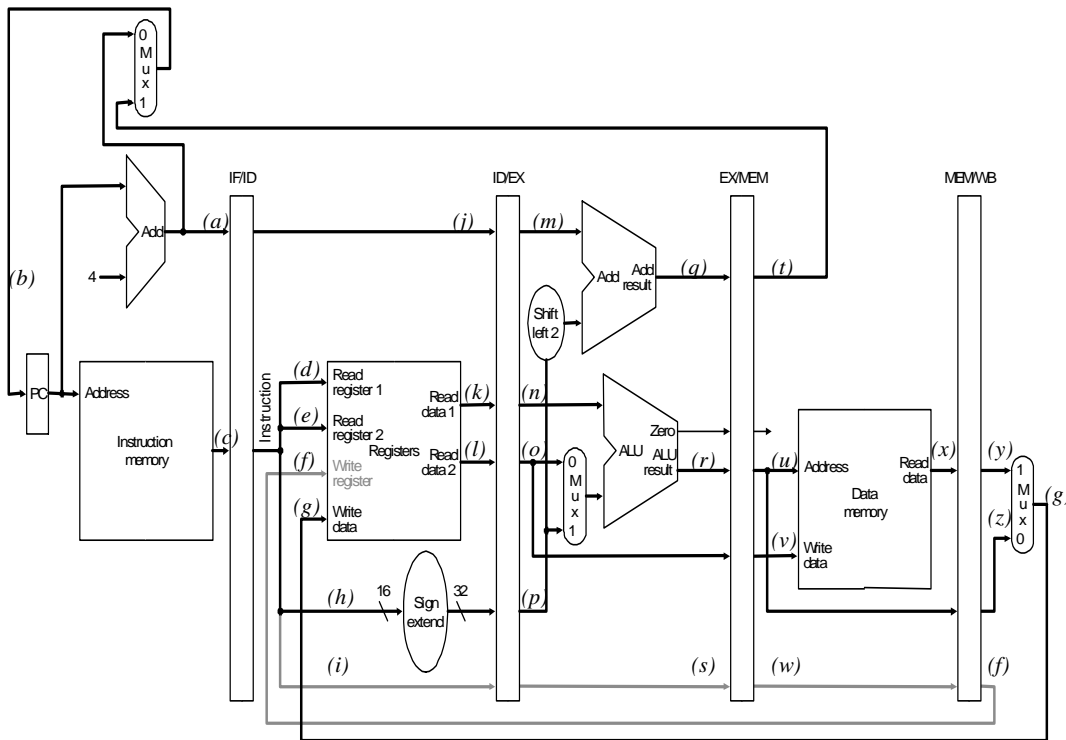
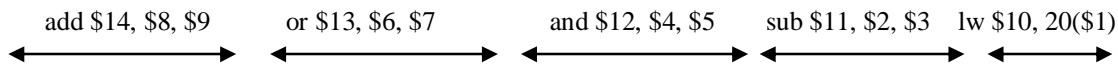
3. The pipelined MIPS starts executing the following five instructions stored in memory addressed from **0x4000000**. Initial register contents are as follows. Assume that all other registers are initialized to zero. At the fifth cycle, each stage of the pipeline executes the instruction shown in the figure. Identify the values for wires in the figure (marked (a)-(z)) **just after the fifth cycle of the execution**.

Instructions executed as well as their binary and hexadecimal representations are as follows (numbers used in instructions are decimal numbers).

lw \$10, 20(\$1)	100011 00001 01010 0000 0000 0001 0100 (0x8c2a 0014)
sub \$11, \$2, \$3	010000 00010 00011 01011 00000 100100 (0x4043 5824)
and \$12, \$4, \$5	010000 00100 00101 01100 00000 100110 (0x4085 6026)
or \$13, \$6, \$7	010000 00110 00111 01101 00000 100111 (0x40c7 6827)
add \$14, \$8, \$9	010000 01000 01001 01110 00000 100000 (0x4109 7020)

Initial register contents are:

\$pc = **0x4000 0000**, \$4 = **0x0000 0400**, \$5 = **0x0000 0500**



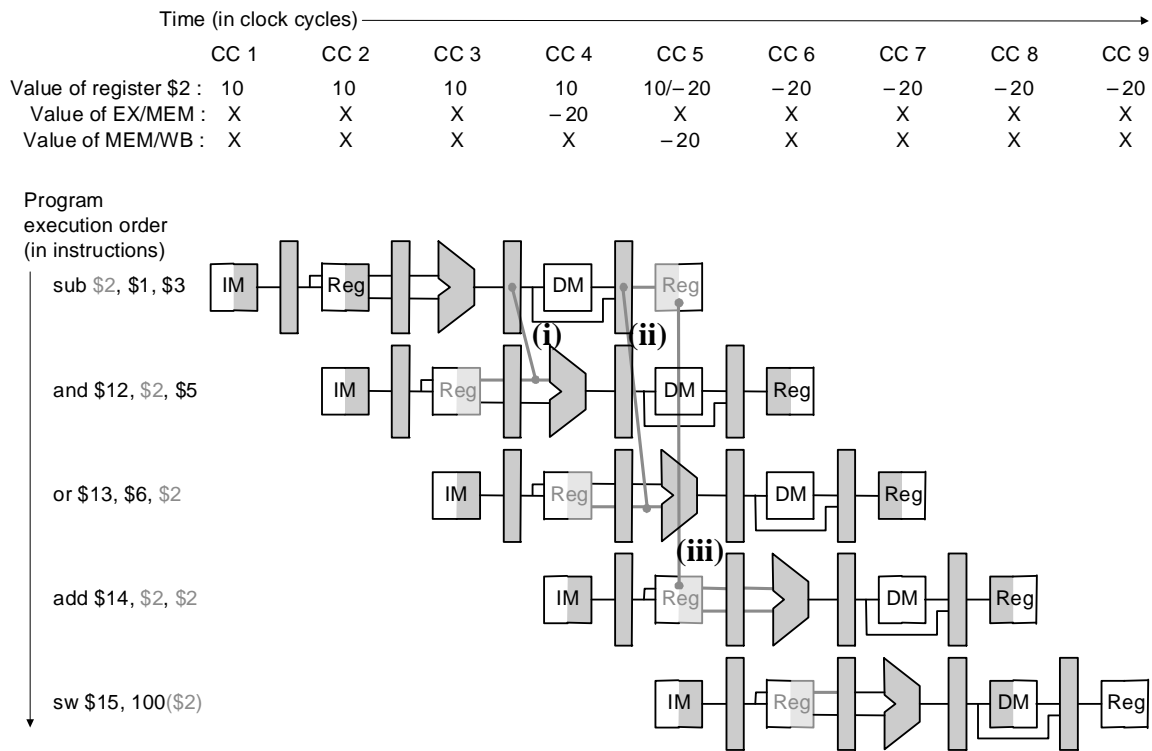
4. As discussed in class, data hazards can be avoided via forwarding and there are four different forwarding cases (Case A~D listed below). Identify the forwarding case for each of the three hazards (i, ii and iii in the figure below).

- Case A: EX/MEM.RegisterRd = ID/EX.RegisterRs
- Case B: EX/MEM.RegisterRd = ID/EX.RegisterRt
- Case C: MEM/WB.RegisterRd = ID/EX.RegisterRs
- Case D: MEM/WB.RegisterRd = ID/EX.RegisterRt

Data hazard (i): Data forwarding case A, B, C, D, or anything else?

Data hazard (ii): Data forwarding case A, B, C, D, or anything else?

Data hazard (iii): Data forwarding case A, B, C, D, or anything else?



5. The following sequence of MIPS instructions is executed in the pipelined architecture.

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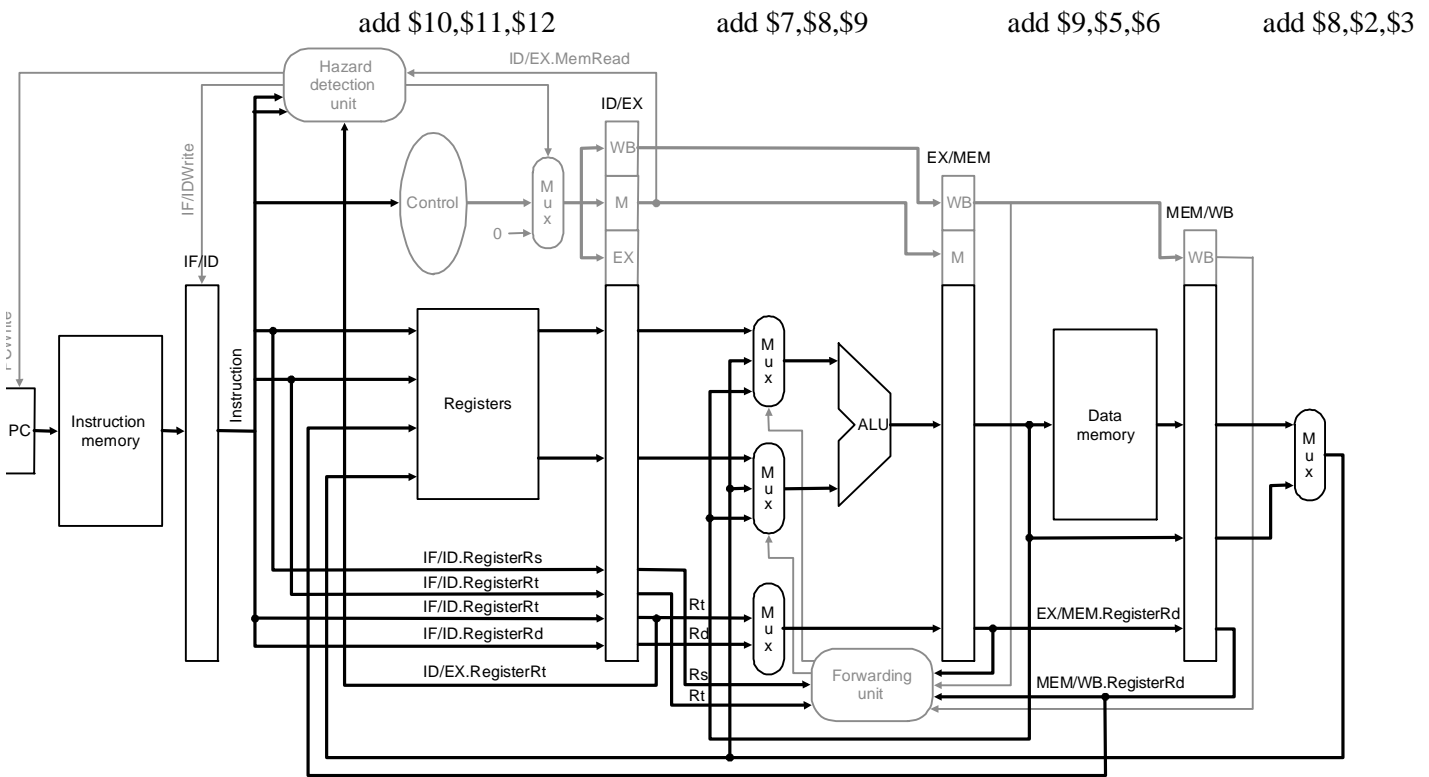
add $8, $2, $3
add $9, $5, $6
add $7, $8, $9
add $10, $11, $12
add $13, $14, $15
    
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(i) During the fifth cycle of execution, determine the followings.

- ID/EX.Rs =
- ID/EX.Rt =
- EX/MEM.Rd =
- MEM/WB.Rd =

(ii) Which comparisons are being made by the forwarding unit during the fifth cycle of execution? (e.g., 4 = 5 ?)

(iii) Identify the forwarding datapath(s) that is (are) activated during the fifth cycle of execution by marking connections on the two muxes before the main ALU. (e.g., )



## Homework #2 (Due Thr, Sep. 27) EEC 581, Fall 2007

1. Here is a series of address references: 0x18, 0x41, 0x82, 0x143, 0x401, 0x14b. Assume a direct-mapped cache with eight blocks (block number 0~7) that is initially empty. Block size is 16 bytes (0x10 bytes).

When the first memory address 0x18 is referenced, it must be a cache miss because the cache is initially empty. Therefore, the corresponding 16-byte memory block (memory address 0x10~1f) is brought into cache. And it will be positioned in Block 1 in the cache as in the following diagram.

Block 0	Block 1	Block 2	Block 3	Block 4	Block 5	Block 6	Block 7
	0x10~1f						

(a) When the next memory address 0x41 is referenced, it is also a cache miss because the corresponding memory block (0x40~4f) is not found in the cache, either. Show how the cache contents change in the following diagram. (Hint: Block 1 continues to have the same contents as in the above.)

Block 0	Block 1	Block 2	Block 3	Block 4	Block 5	Block 6	Block 7

For the subsequent memory references, determine whether it is a cache hit or miss and mark the changes of the cache in the diagram. (Hint: If it is a cache hit, there would be no change in the cache.)

(b) For memory reference 0x82: Hit or Miss?

Block 0	Block 1	Block 2	Block 3	Block 4	Block 5	Block 6	Block 7

(c) For memory reference 0x143 (Hint: 0x143 is a hexadecimal number): Hit or Miss?

Block 0	Block 1	Block 2	Block 3	Block 4	Block 5	Block 6	Block 7

(d) For memory reference 0x401: Hit or Miss?

Block 0	Block 1	Block 2	Block 3	Block 4	Block 5	Block 6	Block 7

(e) For memory reference 0x14b: Hit or Miss?

Block 0	Block 1	Block 2	Block 3	Block 4	Block 5	Block 6	Block 7

2. Consider the memory system with the following properties:

Cache (direct mapped cache):

- Cache size 256 bytes, block size 16 bytes ( $2^4$  bytes)
- Tag/Valid bits for cache blocks are as follows.

Block index	Tag	Valid	Cache block data
0	0	1	
1	2	0	
2	2	0	
3	0	1	
4	1	0	
5	3	0	
6	3	0	
7	1	1	<i><b>Data is not shown</b></i>
8	2	0	
9	1	0	
a	3	1	
b	2	1	
c	0	0	
d	2	1	
e	1	0	
f	3	0	

(a) For a memory reference 0x176, write the address in 11-bit binary format.

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(b) What are the tag, block index and block offset for the memory reference?

(c) Is it a cache hit or miss?

3. Consider a virtual memory system with the following properties:

Virtual memory:

- Virtual memory size 2048 bytes ( $2^{11}$  bytes, address range 0~0x7ff)
- Physical memory size 1024 bytes ( $2^{10}$  bytes, address range 0~0x3ff)
- Page size 256 bytes ( $2^8$  bytes)
- Page table entries (PPN/Valid) are as follows (on the left).

VPN	PPN	Valid
0	2	0
1	2	1
2	1	0
3	0	1
4	3	0
5	2	0
6	2	0
7	1	1

VPN	PPN	Valid
7	1	1
1	2	1

TLB:

- 2 TLB entries (VPN/PPN/Valid) are as in the above (on the right).

Cache (direct mapped cache):

- Cache size 128 bytes, block size 16 bytes ( $2^4$  bytes)
- Tag/Valid bits for cache blocks are as follows.

Block index	Tag	Valid	Cache block data
0	0	1	
1	6	0	
2	7	0	
3	0	1	<i><b>Data is not shown</b></i>
4	5	0	
5	3	0	
6	3	0	
7	3	1	

(1) For the virtual memory reference 0x7f6, answer the followings.

(a) Write the address in 11-bit binary format.

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(b) What are the virtual page number and page offset in hexadecimal format?

(c) What are the physical page number and the physical memory address in hexadecimal format?

(d) What are the tag, block index and block offset?

(e) Is it TLB hit/miss/NA? (f) Is it page table hit/miss/NA? (g) Is it cache hit/miss/NA?

(2) For the virtual memory reference 0x133, answer the followings.

(a) Write the address in 11-bit binary format.

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(b) What are the virtual page number and page offset in hexadecimal format?

(c) What are the physical page number and the physical memory address in hexadecimal format?

(d) What are the tag, block index and block offset?

(e) Is it TLB hit/miss/NA? (f) Is it page table hit/miss/NA? (g) Is it cache hit/miss/NA?

(3) For the virtual memory reference 0x309, answer the followings.

(a) Write the address in 11-bit binary format.

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(b) What are the virtual page number and page offset in hexadecimal format?

(c) What are the physical page number and the physical memory address in hexadecimal format?

(d) What are the tag, block index and block offset?

(e) Is it TLB hit/miss/NA? (f) Is it page table hit/miss/NA? (g) Is it cache hit/miss/NA?

(4) For the virtual memory reference 0x452, answer the followings.

(a) Write the address in 11-bit binary format.

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(b) What are the virtual page number and page offset in hexadecimal format?

(c) What are the physical page number and the physical memory address in hexadecimal format?

(d) What are the tag, block index and block offset?

(e) Is it TLB hit/miss/NA? (f) Is it page table hit/miss/NA? (g) Is it cache hit/miss/NA?

4. Fill in the blanks in the following cache-virtual memory interaction. Answer “N/A” if there is no such a case.

TLB	Page table	Cache	Activity upon a memory read
Hit	Hit	Hit	Translate virtual address to physical address. Read data from cache.
Hit	Hit	Miss	(a)
Hit	Miss	Hit	(b)
Hit	Miss	Miss	(c)
Miss	Hit	Hit	(d)
Miss	Hit	Miss	Read page table to translate virtual address. Bring a memory block into cache. Read data from cache.
Miss	Miss	Hit	N/A
Miss	Miss	Miss	(e)

**Homework #3 (Due Thr, Oct. 11)**  
**EEC 581, Fall 2007**

1. Exercise 2.2
2. Exercise 2.3
3. Exercise 2.7
4. Exercise 2.11

**Homework #4 (Due Thr, Nov. 15)**  
**EEC 581, Fall 2007**

1. Exercise 4.1
2. Exercise 4.2
3. Exercise 4.3
4. Exercise 4.7
5. Exercise 4.14

**Homework #5 (Due Thr, Dec. 6)**  
**EEC 581, Fall 2007**

1. Exercise 5.1
2. Exercise 5.6