

Homework #1 (Due Mon, Sep. 17) EEC 485, Fall 2007

1. Exercise 7.9
2. Exercise 7.10
3. Exercise 7.12
4. Exercise 7.16

Homework #2 (Due Wed, Oct. 3) EEC 485, Fall 2007

1. Exercise 7.29
2. Exercise 7.35
3. Exercise 7.39
4. Exercise 7.40

Homework #3 (Due Mon, Oct. 22) EEC 485, Fall 2007

1. Three basic components in a processor are registers, ALU and memory. They need to be interconnected (called datapath) to perform an instruction as shown in Figure 1 but the required connections vary depending on the instruction to be executed. Identify the connections among (a)-(h) for executing the following instructions as in the example (“lw” instruction) below.

lw \$2, 100(\$3)	needs datapath connections (a, b, c, g, h)
sw \$4, 100(\$5)	needs datapath connections ()
slt \$5, \$6, \$7	needs datapath connections ()
beq \$5, \$6, label	needs datapath connections ()

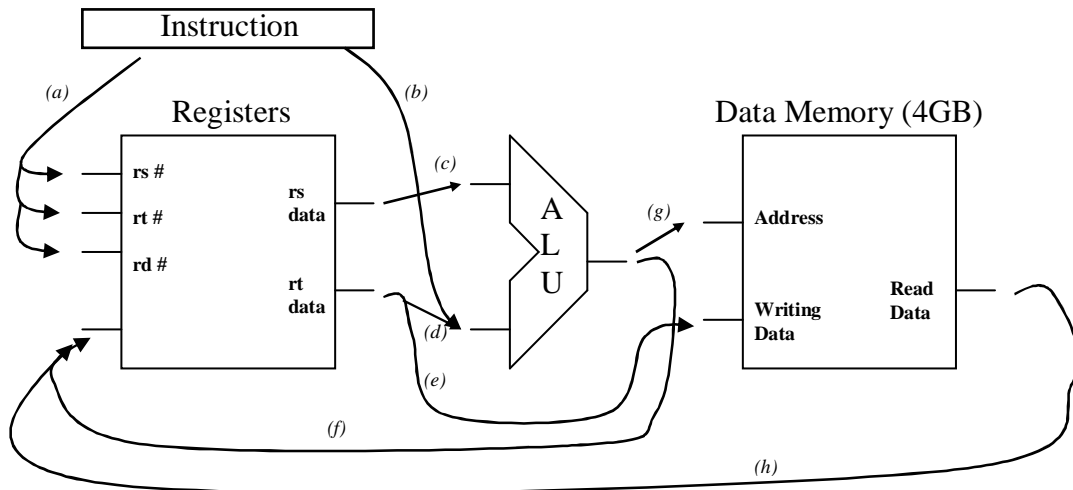


Figure 1

2. Give values on data path connections (a)-(f) in Figure 2, which will be used when executing “add \$8, \$4, \$7” instruction. Content of registers are: [\$4]=0x00004444, [\$8]=0x88880000, and [\$7]=0x77770000. For all values, make sure to write the number with the correct size; e.g. “0x0008” represents 16-bit number 8.

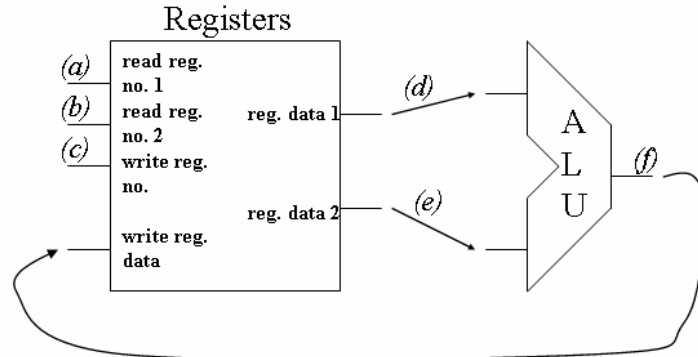


Figure 2

3. Consider the single-cycle implementation of MIPS as in Figure 3, where the highlighted are active parts of the datapath when it executes “sw \$7, 4(\$4)”. The content of registers are \$4 = 0x00004444, \$7 = 0x77770000. Identify the values that each highlighted line carries while executing the sw instruction. Assume that the store-word instruction is stored in memory address of 0x6000 0000.

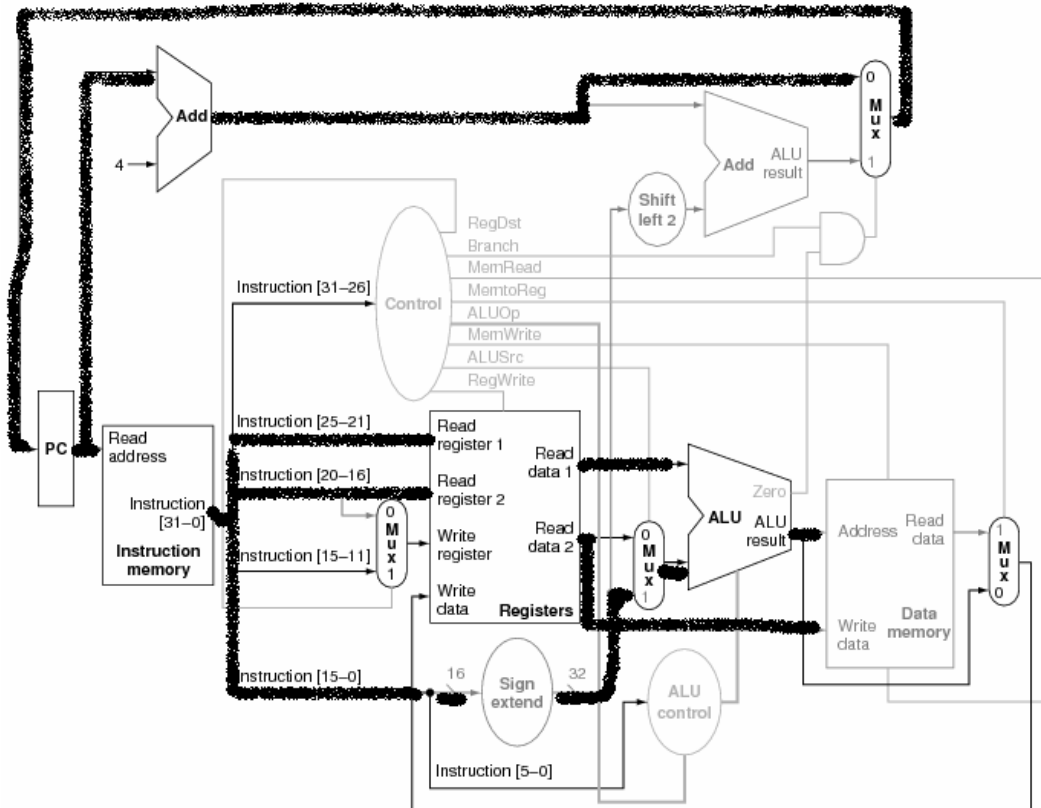
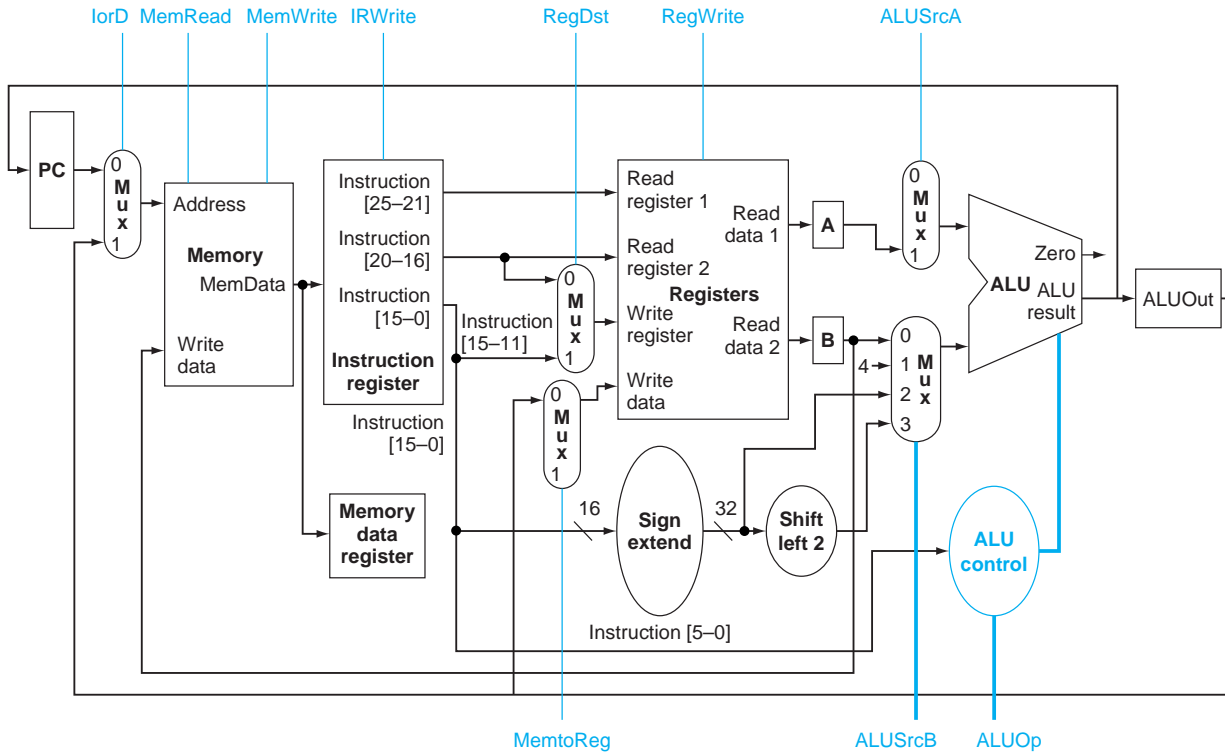


Figure 3: Single cycle implementation of MIPS CPU.

4. Figure 4 shows the multicycle implementation of MIPS CPU. List the control signals generated during the execution of an “sw” instruction.



Cycle	RTL	Write control signals	ALUOp1/ALUOp0	Multiplexor selectors
Instruction fetch	IR = Memory [PC] PC = PC + 4			
Instruction decode/register fetch	A = Reg [IR[25-21]] B = Reg [IR[20-16]] ALUOut = PC + (sign-extend (IR[15-0]) << 2)			
Address computation	ALUOut = A + sign-extend (IR[15-0])			
Memory access	Memory[ALUOut]= B	MemWrite		IorD = 1

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Figure 4: Multi-cycle implementation of MIPS CPU and its RTL description/control signals when executing “sw” instruction.

Homework #4 (Due Wed, Oct. 31)
EEC 485, Fall 2007

1. Exercise 6.3
2. Exercise 6.4
3. Exercise 6.5
4. Exercise 6.6
5. Exercise 6.7

Homework #5 (Due Wed, Nov. 21)
EEC 485, Fall 2007

1. Exercise 6.14
2. Exercise 6.15
3. Exercise 6.20
4. Exercise 6.22
5. Exercise 6.23