

EEC 485 High Performance Architecture, Fall 2007

Date	Content	Reading Assignments	Assignment Due
Aug 27 M	Introduction		
Aug 29 W	7.1 Memory hierarchy	Section 7.1	
Sep 3 M	NO CLASS (Labor Day)		
Sep 5 W	7.2 The basics of caches	Section 7.2	
Sep 10 M	7.2 The basics of caches	Section 7.2	
Sep 12 W	7.3 Improving cache performance	Section 7.3	
Sep 17 M	7.3 Improving cache performance	Section 7.3	Homework #1
Sep 19 W	NO CLASS		
Sep 24 M	7.4 Virtual memory	Section 7.4	Project #1
Sep 26 W	7.4 Virtual memory	Section 7.4	
Oct 1 M	7.5~6 Memory hierarchy framework & Pentium	Section 7.5~6	
Oct 3 W	7.5~6 Memory hierarchy framework & Pentium	Section 7.5~6	Homework #2
Oct 8 M	NO CLASS (Columbus Day)		
Oct 10 W	5. Multicycle processor: Data path and control	Ch. 5 (review)	
Oct 12 F	Project presentation		Project #2
Oct 15 M	6.1 An overview of pipelining	Section 6.1	
Oct 17 W	Midterm Exam		
Oct 22 M	6.2 A pipelined datapath	Section 6.2	Homework #3
Oct 24 W	6.3 Pipelined control	Section 6.3	
Oct 29 M	6.3 Pipelined control	Section 6.3	
Oct 31 W	6.4 Data hazards and forwarding	Section 6.4	Homework #4
Nov 5 M	6.5 Data hazards and stalls	Section 6.5	
Nov 7 W	6.5 Data hazards and stalls	Section 6.5	Project #3
Nov 12 M	NO CLASS (Veteran's Day)		
Nov 14 W	6.6 Branch hazards	Section 6.6	
Nov 19 M	6.6 Branch hazards	Section 6.6	
Nov 21 W	6.8 Exceptions	Section 6.8	Homework #5
Nov 26 M	8.1~2 I/O performance, Networks, Busses	Section 8.1~2	
Nov 28 W	8.5~7 Interfacing and designing I/O devices	Section 8.5~7	
Nov 30 F	Project presentation		Project #4
Dec 3 M	9.1~2 Multiprocessors	Section 9.1~2	
Dec 5 W	9.3 Single-bus multiprocessors	Section 9.3	
Dec 14 F	Final Exam (0830-1030 AM)		