

EEC 485 High Performance Architecture, Fall 2008

Date	Content	Reading Assignments	Assignment Due
Aug 26 T	Introduction		
Aug 28 R	2~3. Instruction set architecture	Ch. 2&3 (review)	
Sep 2 T	5. Multicycle processor: Data path and control	Ch. 5 (review)	
Sep 4 R	6.1 An overview of pipelining	Section 6.1	
Sep 9 T	6.2 A pipelined datapath	Section 6.2	Homework #1
Sep 11 R	6.3 Pipelined control	Section 6.3	
Sep 16 T	6.3 Pipelined control	Section 6.3	
Sep 18 R	6.4 Data hazards and forwarding	Section 6.4	Project #1
Sep 23 T	6.5 Data hazards and stalls	Section 6.5	Homework #2
Sep 25 R	6.5 Data hazards and stalls	Section 6.5	
Sep 30 T	6.6 Branch hazards	Section 6.6	
Oct 2 R	6.6 Branch hazards	Section 6.6	
Oct 7 T	6.8 Exceptions	Section 6.8	Homework #3
Oct 9 R	Project presentation		Project #2
Oct 14 T	No CLASS		
Oct 16 R	Midterm Exam		
Oct 21 T	Review of Midterm Exam		
Oct 23 R	7.1~3 Memory	Ch. 7 (review)	
Oct 28 T	7.4 Virtual memory	Ch. 7 (review)	Homework #4
Oct 30 R	8.1~2 I/O performance,	Section 8.1~2	
Nov 4 T	8.3~4 Networks, Busses	Section 8.3~4	
Nov 6 R	8.5~7 Interfacing and designing I/O devices	Section 8.5~7	Project #3
Nov 11 T	NO CLASS (Veteran's Day)		
Nov 13 R	9.1~2 Multiprocessors	Section 9.1~2	Homework #5
Nov 18 T	9.3 Single-bus multiprocessors	Section 9.3	
Nov 20 R	9.4~6 Distributed memory multiprocessors	Section 9.4~6	
Nov 25 T	9.7 Chip multiprocessors	Section 9.7	
Nov 27 R	NO CLASS (Thanksgiving)		
Dec 2 T	Review		
Dec 4 R	Project presentation		Project #4
Dec 9 T	Final Exam (4-6 PM)		