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NONLINEAR DIGITAL CONTROL IMPLEMENTATION FOR A DC-TO-DC POWER CONVERTER

Jack Zeller, Minshao Zhu, Tom Stimac and Zhiqiang Gao

The Advanced Engineering Research Laboratory
ECE Department, Cleveland State University
Cleveland, OH, USA 44115

ABSTRACT

Closed loop control studies of a DSP-based H-bridge power converter are discussed. The experimental test facility and the analytical development tools being used are described. Open loop modeling results for the NASA-provided power converter test unit are summarized. The performance benefits of nonlinear control algorithms, readily implemented in DSP software, are discussed. Technology issues, specific to the CSU digital control structure are identified and their ongoing development studies are discussed.

INTRODUCTION

Cleveland State University is involved with research to study how the application of direct digital control to spacecraft power converters could enhance their performance and reliability as well as that of complete power management and distribution (PMAD) systems [1]. The work is being conducted by a team of faculty members and students (both graduate and undergraduate) from CSU's Electrical and Computer Engineering (ECE) department. This paper is intended to provide an overview of the entire research activity while focusing on early closed loop control performance results that have been obtained using nonlinear controller algorithms.

To provide background information for readers, the paper begins with a discussion of the objectives for conducting this specific research. This is followed by a brief description of the experimental facility being used to conduct the research. A more detailed description can be found in [2]. Next there will be a description of how the facility was used to experimentally determine linear model representations of the power converter provided by NASA for this program. These linear models [3] serve as the basis for analytically studying a variety of closed loop voltage regulation control strategies. These strategies involve nonlinear control laws that depend upon a digital controller's computational capabilities for their implementation. The main section of the paper will present initial performance results obtained with these digital control strategies. Both simulation and hardware test results will be included and discussed. The final section will: 1) discuss power converter digital control technology areas which warrant further study, and 2) describe DSP control hardware development activities intended to provide tools for broader PMAD control investigations.

RESEARCH OBJECTIVES

Reliable, efficient, well-regulated DC-to-DC power conversion equipment is critical for mission success on most space platforms. As platforms, especially manned spacecraft, become more sophisticated, reliable operation of complete power management and distribution (PMAD) systems becomes a must. As a result there is much interest in determining how and in what areas a more intelligent and robust control structure might be of value. Replacing the present analog control solution with a digital computer based control is one approach toward satisfying this need.

Much work in digital control of DC-to-DC power converters has already been accomplished and documented ([10]-[16]). Either microcontroller-based or DSP-based approaches have been used to realize sophisticated and/or flexible control algorithms, such as PID, Fuzzy Logic, Adaptive Fuzzy, and Feedforward Control. The versatility provided by software programmable digital controllers is well suited to the increasing control performance and reliability demands being placed on new space borne power converters and PMAD systems. Applying previous experience by CSU researchers on highly nonlinear control strategies [5] is the focus of the work to be reported in this paper. One objective of the CSU research will be to evaluate the closed loop performance benefits that these new nonlinear algorithms can bring to DC-to-DC power converters. In addition our DSP-based research will be

conducted so as to evaluate a multitude of control opportunities that can only be accomplished digitally. One example will be the ability to use variable PWM frequency as a method of improving low power converter efficiency. Early results of our studies as well as details of the multitude of ongoing efforts will be discussed in the following sections.

CSU RESEARCH FACILITY

In order to provide an effective research environment, CSU's ECE department allocated one of its laboratories to this project to function as a combined laboratory and office in which to conduct this research. This facility has been designated as the Advanced Engineering Research Laboratory (AERL). In order to conduct realistic experimental research, NASA provided to CSU a Westinghouse-designed 1 KW "brassboard" power converter. This SMPS unit was designed to accept an input voltage between 100 and 160 volts DC and provide a regulated and isolated output DC voltage of 28 volts for loads up to 36 Amps. Galvanic voltage isolation was obtained with a stepdown (3:1) transformer whose primary winding was pulse-width-modulated (PWM) with an H-bridge switching configuration of power MOSFET transistors. The lower voltage secondary winding was rectified and filtered to provide the 28 volt DC output. Pulse-width-modulation (PWM) of the switching devices was used to accomplish closed loop voltage regulation. The analog PWM generation circuitry and analog controller circuitry were removed, since the intent of the research is to accomplish these two functions digitally.

It was decided that a DSP-based digital system would be used rather than a microcontroller approach. Equipment needed to support this approach was put into place and configured to realize a versatile research environment. The DSP development system selected was dSpace Inc.'s [4] rapid-prototyping development system. This system is equipped with a high-performance TI DSP chip, A/D conversion capability as well as digital I/O circuitry. To expedite the development and evaluation of digital control strategies, Mathwork's Matlab/Simulink/Real-Time Workshop toolbox software was selected. Simulink provides the ability to model and accurately simulate the transient performance of dynamic processes to arrive at a set of acceptable closed loop control strategies. Mathworks' Real-Time Workshop will convert a controller, modeled in Simulink, into 'C" code which will run on dSpace's DSP processor to control actual experimental hardware (in this case the 1 KW Westinghouse power converter). This is termed hardware-in-the-loop simulation. The control laws can also be programmed in native "C" code. Then dSpace's compiler and libraries will be used to generate the code for the TI DSP chip on dSpace's processor board. This second approach has been found to generate faster operating real-time control code.

A decision was made early in the program to generate the two-phase PWM signals needed by the H-bridge outside of the DSP by using a programmable CPLD chip. This will off-load a potentially heavy computational burden from the DSP controller. A block diagram of this experimental configuration is shown in Figure 1.

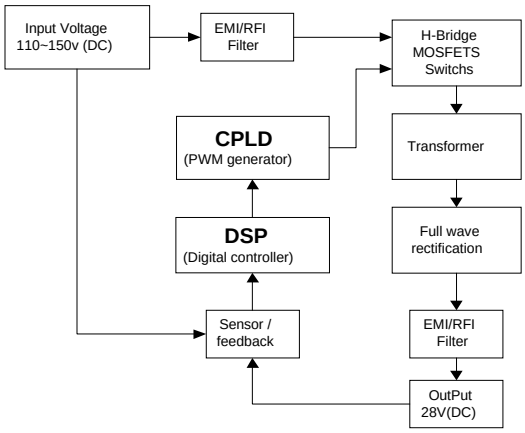

Figure 1: Experimental Facility Block Diagram Description

To complete the experimental research facility, appropriate test equipment was acquired. This included: power supplies, signal generators, digital voltmeters, digital oscilloscopes, and an electronic load bank. The photograph in Figure 2 shows how this array of equipment is configured in our facility. A more detailed description of all of this equipment is included in [2].

Figure 2. Photograph of AERL Experimental Equipment

Linear Model Development

To expedite the analytical control development studies, a linear (transfer function) model of the power converter process was developed. Obtaining the data for this model was the first research activity which used the AERL experimental hardware-in-the-loop configuration. A methodology for using a CPLD device to generate the PWM signals needed to drive the switching converter's gate circuitry was developed. The DSP's algorithmic logic needed to accept a variable pulse width control input and compute the outputs for the CPLD's input registers was configured for evaluation in Simulink. The RTW toolbox was used to convert the simulated algorithmic logic into dSpace's DSP "C" code equivalent [6].

I*t should be noted that the initial design of the algorithm chose an eight (8)bit quantization level for each phase of the*

CPLD's PWM output. Thus the 28 volt DC output could only be resolved to 0.156 volts, (at 120 volts of input). This quantization has proven to be a performance limitation to the control studies and improvements are being evaluated. A brief discussion of the early results of these improvements will be presented later in this paper.

Using the hardware-in-the-loop experimental configuration of Figure 1 and the just-described PWM generation software, linear model data was obtained. By varying the input pulse count, the converter's open loop steady-state performance under varying output current (I_l) load levels and for a range of input supply voltages (V_{in}) was determined. The detailed results of this steady-state mapping can be found in [3]. Using those results, an equation was determined [3] which analytically defines the converter's steady-state output voltage over a range of conditions.

$$V_o = \frac{V_{in}}{(3*256)}(PulseCount) - 0.8 - (0.075*I_L) \quad (1)$$

In (1) the division of the input voltage by 3 accounts for the 3:1 turns ratio of the isolation step-down transformer. The 256 factor is the maximum pulse count due to the eight bit quantization used in the initial design. The 0.8 volts accounts for the rectifier's diode drop while the 0.075 is the approximate output impedance of the converter under load. Eq.(1) can be rearranged to yield a pulse count value which would be needed to produce a particular output voltage knowing the input DC voltage and the load current. This relationship is defined as (2) below: (2)

$$PulseCount = [V_o + 0.8 + 0.075 * I_L] * (3 * 256) / V_{in}$$

The next experimental modeling activity of [3] was to determine the transient behavior of the converter process when subjected to disturbance inputs in: 1) pulse count, 2) load current, and 3) input DC supply voltage. Step inputs in each of these three parameters were used to produce time response data. Curve fit approximation's to this data were used to determine linear transfer function models. The details of the testing activity are included in [3]. The result of this activity was the open loop process transfer function block diagram of Figure 3.

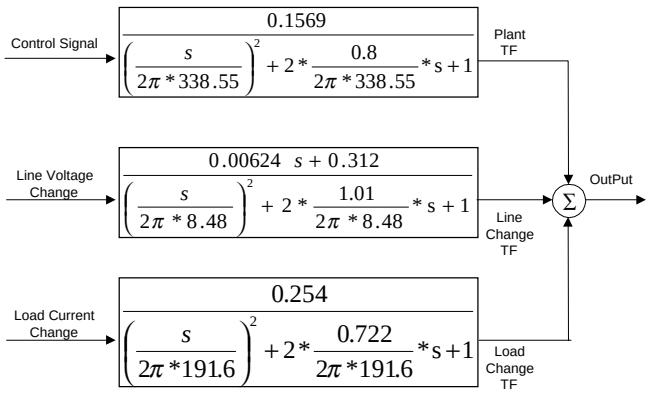

Figure 3 Linear Model Block Diagram

CLOSED LOOP PERFORMANCE RESULTS

Simulink Setup -The results of the simulation studies were obtained using a detailed Simulink model of the digitally controlled converter. The simulation includes the open loop converter model of Figure 3. A comparison of a traditional linear PID control and a nonlinear control (NPID) was performed. Figure 4 shows this model and includes blocks for the two control laws as well as a soft-start feature. Figures 4a-4d are block descriptions of the Simulink subsystems of Figure 4.

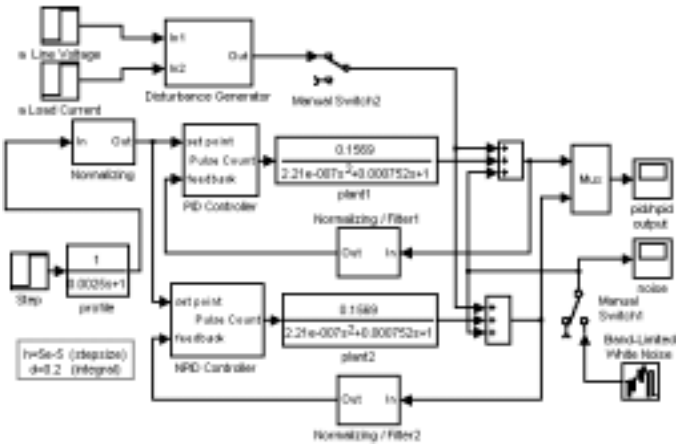

Figure 4 Simulink Simulation Block Diagram

We use a zero-order hold with a sampling period of 50us. The quantizer is used to mimic the dSpace's 12 bitA/D converter. It is set 0.0048828125.

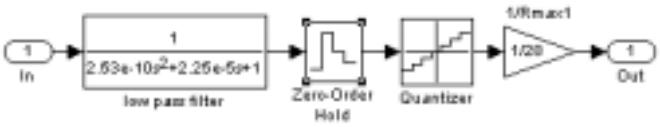

Figure 4a Normalizing and Filtering Subsystem

After comparing the setpoint and feedback signals, the control algorithm is executed and a control signal is produced. It is then converted to a pulse count and sent to the PWM

generator to create real PWM control signals for the switching MOSFET's gate drivers.

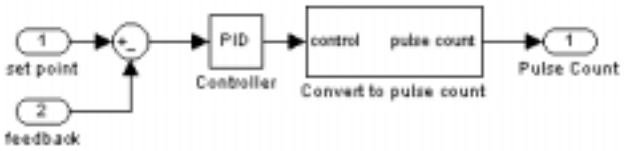

Figure 4b PID Controller Subsystem

The disturbance block in Figure 4c is used to simulate the effects of the Line voltage change and Load current change on the output voltage. It allows us to observe the disturbance rejection performance for each controller. It comes from Figure 3.

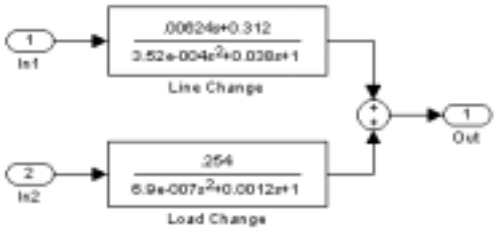

Figure 4c Disturbance Generator Subsystem

The Conversion to pulse count block is shown in Figure 4d, where the saturation limits are set at 0 and 1, respectively. This is because our PWM generator range is 0 - 240 pulse counts. The quantization level in the Quantizer is set at 1.

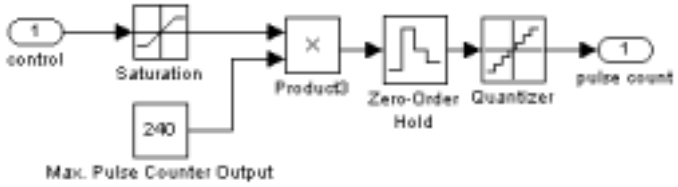

Figure 4d Conversion to Pulse Count Subsystem

NONLINEAR PROPORTIONAL AND INTEGRAL CONTROL

The initial results of the digitally controlled converter using standard Proportional-integral (PI) controller, which is primarily an integral control, have been reported in [2]. Recently, a set of high performance Nonlinear PID control algorithms have been reported [5] and some of them are used here as shown in Figure 4e, which shows the details of the Nonlinear PI block in Figure 4.

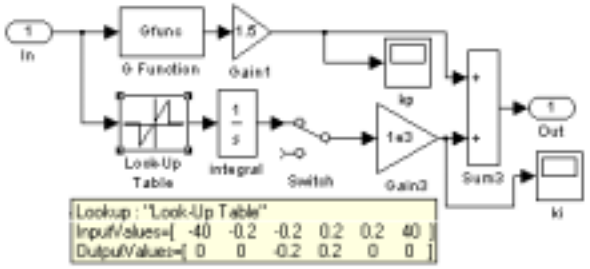

Figure 4e Nonlinear PI Control subsystem

The G-function is Figure 4e is a nonlinear gain function shown in Figure 5, where the green line is normal linear gain and the blue line represents the nonlinear G function. The design philosophy is fully explained in [5]. Here, the intuition is that the gain should be higher when the error is smaller, which makes the controller "more stiff". That is the proportional control is made more sensitive to the small errors. This will also reduce the reliance on the integral control to eliminate steady state errors. Note that the instability is often caused by the 90 degree phase lag in the integral control.

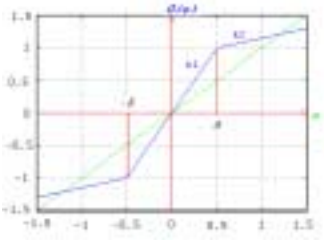

Figure 5 G-Function

It is mathematically expressed as:

$$G(e)=\begin{cases} k_2 * e + (k_1 - k_2) * \delta * \mathrm{sgn}(e) & |e| > \delta \\ k_1 * e & |e| \le \delta \end{cases} \quad (3)$$

Although the use of this nonlinear gain provides good disturbance rejection and stability robustness, it may make the controller too sensitive to noise. Therefore, a compromise is made between the nonlinear proportional control and a limited nonlinear integral control. In particular, the integral term is reformulated as

$$k_i * \int G_i(e)dt \qquad G_i(e)=\begin{cases} 0 & |e| > \delta_i \\ e & |e| \le \delta_i \end{cases} \quad (4)$$

That is, the integrator only integrates when the error is "small", typically when the output is within 10% of the set point.. This design strategy allows the control to effectively avoid undesirable overshoots and the integrator wind-up during large disturbances.

Simulation : Transient Results – Figure 5 show a comparison of the transient performance simulation results obtained for a well-tuned linear PID versus a nonlinear PI control. Figure 5(a) contains results for the application of a 20 Amp load while Figure 5(b) shows results for PWM pulse Count (control variable) respectively. The blue curves are for the PID and the green traces are for the nonlinear PI. The nonlinear controller shows a much smaller deviation from steady-state than the linear PID. Also the nonlinear algorithm is faster.

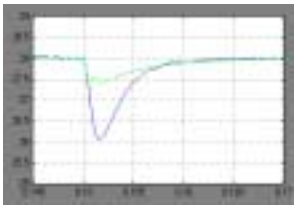

Figure 5(a).Load Transient

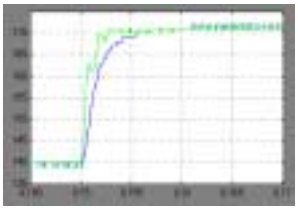

Figure 5(b)PWM pulse Count

Experimental Controller Setup –The two control algorithms were then coded in native "C" code , compiled and down loaded to the DSP system. This code could then operate the converter hardware. After extensive experimentation and tuning activity, transient performance comparison results were obtained. The use of dSpace's Control Desk software helped expedite this tuning activity. Figure 6 is a sample of what the computer screen looks like when Control Desk is employed. The designer has a great deal of critical parameter information available at a glance along with the captured transient data. Even though the actual values may not be readable in the paper, the figure is included to show the capability of the Control Desk software for enhancing productivity.

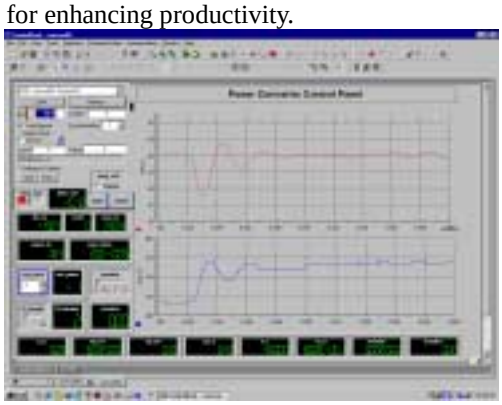

Figure 6 Sample Control Desk Screen

Experimental Transient Results – The transients caused by a sudden change in the load current were captured as was done during the simulation studies.

We used the Control Desk to assist the controller tuning and transient response monitoring. In the following figures, the top trace is Output Voltage, the lower trace is CPLD PWM pulse Count (control signal).

In the hardware test, the load current was changed from 3A to 20A. The lowest load is set 3A so that the inductor in the converter is in continuous conduction.

1) Linear PI (LPI) Controller resluts

The parameter for Linear PI Controller setting are :

$$K_p = 0.2, K_i = 423$$

And the response is shown in Figure 7, which indicates a 15.2ms recovery time and 3.4V peak-to-peak voltage variation.

2) Two-slope Nonlinear PI (NPI) Controller results

According to (3) and (4), the parameters for the NPI controller setting are set as

$$K_1 = 0.256,\ K_2 = 0.024, \delta = 0.4$$

$$K_i = 400, \delta_i = 0.8$$

and the response is shown in Figure.8, which yields a 5.7 ms recovery time and a 3.25V peak-to-peak voltage variation. Comparing to Figure 7 the NPI transient response performs almost 2 times better on the recovery time.

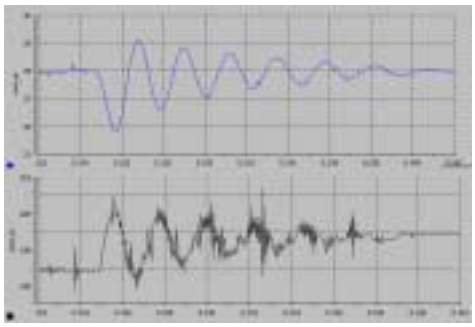

Figure 7 Transient response with Load application(LPI)

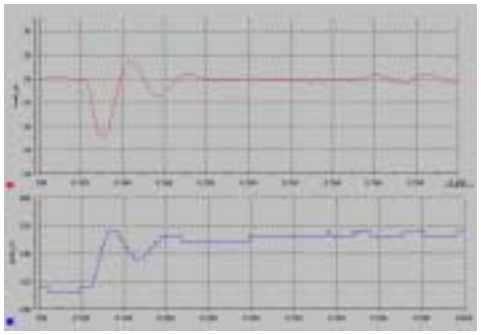

Figure 8 Transient response with Load application(NPI)

The above results show the benefits of using the NPI controller as:

1.Much cleaner control output

2.Much less ringing during load application.

3.Much faster load application recovery time during load application.

ONGOING AND FUTURE RESEARCH PURSUITS

As the AERL team undertook R & D activity to replace the traditional analog SMPS controller with a direct digital solution, a number of technology and system issues became evident. Several of these issues will now be briefly addressed in terms of each one's ongoing design and development activities.

Signal Conditioning – Critical voltage and current variables, which define the converter's performance, must be measured accurately, isolated, and conditioned for sampling by the digital controller. One important aspect of the signal conditioning is the selection of adequate anti-aliasing filters to remove (to filter out) unneeded high frequency information in the measurements. To accommodate these requirements the signal conditioning circuitry was breadboarded for the initial experimental studies. For future control studies, a ruggedized printed circuit version of this circuitry is being designed.

PWM Generation - As stated earlier, CSU's approach to PWM generation is to generate the pulse width gate driving signals with a programmable logic device (CPLD). The present performance limiting eight-bit PWM CPLD will soon be replaced with an alternative CPLD design which provides higher resolution (finer quantization) and will have the ability to vary the PWM frequency directly through commands from the

DSP software. Closed loop control testing of the higher resolution CPLD is now underway. Performance studies using the variable frequency feature will start soon. Results will be reported at a later time.

Control Mode Selection-As was shown in the results section, the new nonlinear control strategies show benefits over linear, more traditional, control modes. It must be noted at this point, however, that the AERL team has not yet implemented a current-mode inner loop. Because we generate the PWM signals digitally, a strategy for effectively using sensed transformer primary current in an inner current loop control has not yet been determined. Resolving this control design issue is a major priority.

DSP Control Development Platform –The dSpace rapid-prototype development equipment has played an invaluable role in our controls research. However, at CSU we are designing an easier-to-use DSP development platform to study converter control in a broader PMAD system context. A major feature of this platform design is the inclusion two high-speed IEEE-1394 (Firewire) data communication ports.

SUMMARY

A research program on direct digital control of power converters has been described. Analytical and experimental results for a new nonlinear control strategy are discussed and compared against traditional linear control modes. The results encourage continued study into nonlinear approaches to converter voltage regulation. Finally some of the technology issues related to digital converter control are identified and efforts for their resolution discussed.

ACKNOWLEDGMENTS

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