"*FPGA Prototyping with SystemVerilog Examples*" Adoption for Digilent Arty A7 Board

Release v1.0 (updated on 05/2018)

1 Overview

The codes in FPGA Prototyping with VHDL Examples are tailored to the I/O peripherals of the Digilent Nexys 4 DDR board. The Arty A7 board has a smaller Artix device and different I/O configuration. However, most designs and FPro systems in the book can be adopted with minor code revisions and with few additional external modules.

The original HDL codes and C++ codes are kept as much as possible and the revised portions are commented and replaced. Several HDL files are revised to accommodate the Arty A7 board. These files are designated with an `_art_a7` postfix and can be found in the arty_supplement folder.

A new MMIO xadc core is developed to match the analog input configuration of the arty board. For the remaining part, the original HDL codes and C++ codes are kept as much as possible and the revised portions are commented and replaced. To minimize the difference, some code segment is not optimal for the Arty A7 board. After having a better comprehension, we can easily modify and clean up the codes to accommodate the Arty board configuration.

This article summarizes the options for the external modules and adaptors and the required code revisions. Digilent manufactures a series of "Arty" boards. Their layouts and basic I/O configurations are similar. Most discussion can be applied to these boards as well.

2 Device and Constraint File

2.1 Artix device

The Arty A7 board uses a smaller Artix-7 device. When creating the project, select the device as follows:

- Family: `Artix-7`
- Package: `csg324`
- Part: `xc7a35ticsg324-1L`

2.2 Constraint (.xdc) file

A new constraint file, `arty_chu.xdc`, is constructed for the Arty A7 board.

3 Revisions of FPro Systems

3.1 Revision of Vanilla FPro System

- Set `N_LED` and `N_SW` to 4 since there are only 4 switches and 4 discrete LEDs on the Arty A7 board:

```
mmio_sys_unit: entity work.mmio_sys_vanilla
generic map(N_LED=>4, N_SW=>4)
```

3.2 Revision of Vanilla-Daisy FPro System

The Arty A7 board does not have a VGA port and must use a "pmod VGA" module, which takes two PMOD ports. In addition, because of the smaller BRAM capacity in an Artix-7 35T device, the frame buffer is removed. The required steps are:

- Set `N_LED` and `N_SW` to 4 in `mmio_sys_vanilla` subsystem.

- Use PMOD JC and PMOD JD for the “pmod VGA” module (shown below).

image source: digilentinc.com

- Use the revised video subsystem, `video_sys_daisy_no_frame`.
- Comment out the frame check routine in the testing program.

3.3 Revision of Sampler FPro System

The Arty A7 board lacks several I/O peripherals of the Nexys 4 DDR board but provides an Arduino-like header. We can route the corresponding signals to the Arduino header or one of the four PMODs. External modules can be added if desired. A new XADC MMIO core is developed to facilitate the Arty A7 configuration. The needed revisions for each MMIO IP core in the Sampler FPro system are summarized below:

- Timer core: no change.
- UART core: no change.
- GPO core for discrete LEDs: no change (the `N_LED` generic is set to 4 at top-level).
- GPI core for slide switches: no change (the `N_SW` generic is set to 4 at top-level).
- XADC core: The XADC configuration on the Arty A7 board is very different. A new MMIO core is constructed and the detail is discussed in a separate section below.
- PWM core: The PWM core is expanded to include 16 channels, in which 12 channels are connected to four tri-color LEDs on Arty A7 board and the other 4 channels are connected to the Arduino headers.
- Debounce core: no change.
- Seven-segment LED core: not used.
- SPI core: The Nexsys board contains an ADXL362 device (an accelerometer) and the SPI core is used to control the device. The Arty A7 board does not have any SPI device and the SPI signals (including a 3-bit slave-select `ss_n` signal) are connected to the Arduino header. Any external modules with SPI interface can be used. If desired, the SPI signals can also be rerouted to a PMOD port of the Arty A7 board. The “pmod ACL2” module from Digilent contains the same ADXL362 device and can be used for testing.
- I2C core: The Nexsys 4 board contains an ADT7420 device (a temperature sensor) and the I2C core is used to control the device. The Arty A7 board does not have any I2C device and the I2C signals are connected to the Arduino header. Any external modules with I2C interface can be used. If desired, the I2C signals can also be rerouted to a PMOD port of the Arty A7 board. The “pmod TMP2” module from Digilent contains the same ADT7420 device and can be used for testing.
- PS2 core: The Arty A7 board does not have a PS2 port. If desired, the PS2 signals can also be rerouted to a PMOD port of the Arty A7 board. A “pmod PS2” module from Digilent can be used to connect a PS2 mouse or PS2 keyboard.
- DDFS core/ADSR core: The Nexsys 4 board routes the PDM audio signal to an active low-pass filter and then to an audio jack. The Arty A7 board does not contain this circuit. The `pdm` signal

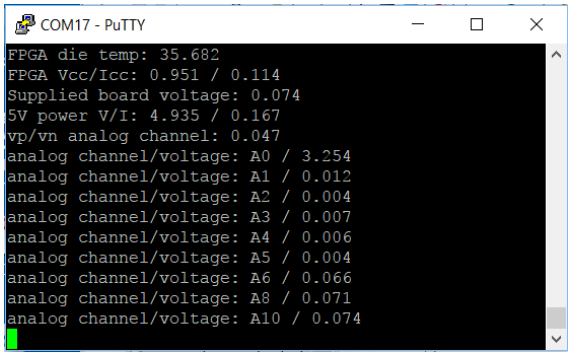
from the DDFS core is connected the lower row of PMOD JA. The "pmod AMP2" module from Digilent contains a simple low-pass filter and a class-D audio amplifier as well as an audio jack. The module can be used instead. The `pdm` and `ddfs_sq_wave` signals are also connected to the Arduino header.

4 XADC MMIO Core

The Nexys 4 DDR board uses 4 channels of Artix's XADC macro cell and connect four pairs of differential analog input signals to the PMOD JXADC. The setup of the Arty A7 is very different. The XADC macro is configured as follows:

- 1 dedicated vp/vn channel
- 6 single-ended channels (pin a0 to a5) of Arduino header
- 3 differential channels (pin a6/a7, a8/a9, and a10/a11) of extended Arduino header
- 4 channels for onboard voltage and current measurement

A new XADC MMIO core, `chu_xadc_arty_a7_core`, is developed to accommodate the Arty A7 board. It retrieves 16 auxiliary analog measurements (3 unused) plus the vp/vn, core temperature, and core voltage readings. A new driver class, `XadcArtyCore`, adds methods to retrieve raw data and convert them to adequate format. A sample screenshot of XADC reading is shown below:



5 Usage

An FPro system can be constructed on the Arty A7 board as follows:

- Download and decompress the zip file that contains the original source codes.
- Decompress the zip file that contains revised files (in `arty_supplement` folder).
- Follow the instruction in the *Organization and Usage of Source Files of "FPGA Prototyping Using SystemVerilog Examples: MCS edition*" article associated with the original source files to construct an FPro system. Replace the revised files (those end with a `_arty_a7` postfix) as needed.

6 Pre-built FPro System

A quick alternative to constructing an FPro system from source files is to import a pre-built Vivado (version v2017.2) project. Three compressed project files incorporate the three FPro systems used in Part II, III, and IV of the book and can be found on the companion website:

- `Arty_sv_vanillia.xpr.zip`: vanilla FPro system of Part II
- `arty_sv_sampler.xpr.zip`: sampler FPro system of Part III
- `arty_sv_video.xpr.zip`: vanilla-daisy FPro system of Part IV

7 Other Arty Boards

Digilent manufactures a series of Arty boards, including Arty A7, Arty S7, and Arty Z7 as well as Pynq. These boards have a similar layout and basic I/O configuration. With some minor modifications, the discussion and codes in the previous sections can be applied to these boards as well.