Adoption for Digilent Basys 3 Board

Release v1.0 (updated on 05/2018)

1 Overview

The codes in FPGA Prototyping with VHDL Examples are tailored to the I/O peripherals of the Digilent Nexys 4 DDR board. The Basys 3 board has a smaller Artix device and fewer onboard peripherals. However, most designs and FPro systems in the book can be adopted with minor code revisions and with few additional external modules.

The original HDL codes and C++ codes are kept as much as possible and the revised portions are commented and replaced. Several HDL files are revised to accommodate the Basys 3 board. These files are designated with a _basys3 postfix and can be found in the basys3_supplement folder.

This article summarizes the options for the external modules and adaptors and the required code revisions.

2 Device and Constraint File

2.1 Artix device

The Basys 3 board uses a smaller Artix-7 device. When creating the project, select the device as follows:

- Family: Artix-7
- Package: cpg236
- Part: xc7a35tcpg236-1

2.2 Constraint (.xdc) file

A new constraint file, basys3_chu.xdc, is constructed for the Basys 3 board. The top-level port names are identical to those of the Nexys 4 DDR board. However, some ports are removed since several I/O peripherals of the Nexys 4 DDR board are not included in the Basys 3 board.

3 Revisions of FPro Systems

3.1 Revision of Vanilla FPro System

- Remove the `reset_n` signal in the top-level design since Basys 3 does not has a dedicated reset button. If needed, a normal pushbutton can be assigned for this purpose.

3.2 Revision of Vanilla-Daisy FPro System

- Remove the `reset_n` signal as in the Vanilla FPro system.
- Remove the frame buffer because of the smaller BRAM capacity in an Artix-7 35T device. The revised video subsystem, `video_sys_daisy_no_frame`, should be used instead.
- Comment out the frame check routine in the testing program.

3.3 Revision of Sampler FPro System

The Basys 3 board lacks several I/O peripherals of the Nexys 4 DDR board. We route the corresponding signals to the PMODs. External modules can be added if desired. The needed revisions for each MMIO IP core in the Sampler FPro system are summarized below:

- Timer core: no change.
- UART core: no change.
- GPO core for discrete LEDs: no change.

- GPI core for slide switches: no change.
- XADC core: Both Nexsys and Basys boards connect 4 XADC channels to a PMOD. However, the channel configurations of the two boards are different. A revised core (chu_xadc_basys3_core) replaces the original core.
- PWM core: The Nexsys board has two tri-color LEDs and 6 channels of the PWM core are connected to the LEDs. The Basys board does not have any. Four PWM channels are connected to the bottom row of PMOD A. An external tri-color LEWD can be used.
- Debounce core: no change.
- Seven-segment LED core: The Nexsys board has an 8-digit 7-segment LED display. The Basys board contains a smaller 4-digit 7-segment LED display. The four MSBs of the enable signal (`an[7 downto 4]`) are left unconnected.
- SPI core: The Nexsys board contains an ADXL362 device (an accelerometer) and the SPI core is used to control the device. The Basys board does not have any SPI device. The SPI signals are connected to the top row of PMOD JB. The "pmod ACL2" module from Digilent contains the same ADXL362 device and can be used for testing. Other external modules with SPI interface can be used as well.
- I2C core: The Nexsys board contains an ADT7420 device (a temperature sensor) and the I2C core is used to control the device. The Basys board does not have any I2C device. The I2C signals are connected to the top row of PMOD JC. The "pmod TMP2" module from Digilent contains the same ADT7420 device and can be used for testing. Other external modules with I2C interface can be used as well.
- PS2 core: no change.
- DDFS core/ADSR core: The Nexsys board routes the PDM audio signal to an active low-pass filter and then to an audio jack. The Basys board does not contain this circuit. The `pdm` signal from the DDFS core is connected the lower row of PMOD JC. The "pmod AMP2" module from Digilent contains a simple low-pass filter and a class-D audio amplifier as well as an audio jack. The module can be used instead.

4 Usage

An FPro system can be constructed on the Basys 3 board as follows:

- Download and decompress the zip file that contains the original source codes.
- Decompress the zip file that contains revised files (in basys3_supplement folder).
- Follow the instruction in the *Organization and Usage of Source Files of "FPGA Prototyping Using SystemVerilog Examples: MCS edition*" article associated with the original source files to construct an FPro system. Replace the revised files (those end with a _basys3 postfix) as needed.

5 Pre-built FPro System

A quick alternative to constructing an FPro system from source files is to import a pre-built Vivado project. Three compressed project files incorporate the three FPro systems used in Part II, III, and IV of the book and can be found on the companion website:

- basys3_sv_vanillia.xpr.zip: vanilla FPro system of Part II
- basys3_sv_sampler.xpr.zip: sampler FPro system of Part III
- basys3_sv_video.xpr.zip: vanilla-daisy FPro system of Part IV