PREFACE

HDL (hardware description language) and FPGA (field-programmable gate array) devices allow designers to quickly develop and simulate a sophisticated digital circuit, realize it on a prototyping device, and verify operation of the physical implementation. As the capacity of FPGA devices continues to grow, a device can accommodate an SoC (system on a chip) design, which integrates a processor, memory modules, I/O peripherals, and custom hardware accelerators into a single chip. This book uses a “learning by doing” approach and illustrates the FPGA and HDL development and design process by a series of examples in the SoC context.

The examples start with simple gate-level circuits, progress gradually through the RT (register-transfer) level modules, and lead to a functional embedded system with custom I/O peripherals and hardware accelerators. A simple SoC framework, FPro (abbreviated from the book title “FPGA Prototyping”), is introduced as a platform to integrate all the design examples together. An FPro system contains a Xilinx MicroBlaze MCS soft-core processor, a video subsystem, and the MMIO (memory-mapped I/O) subsystem that can incorporate custom I/O cores. Except for the processor, all components are designed and coded from scratch. All the hardware and software examples can be synthesized, compiled, and physically tested on the prototyping board.

Focus and audience

Focus The primary focus of this book is on developing efficient and reliable digital systems and effectively using HDL as a tool to describe the intended hardware. The HDL language itself is not the main subject and its coverage is limited to a
small synthesizable subset. The book uses about a dozen proven code templates to provide the skeletal structures of various types of circuits. These templates are general and can easily be integrated to construct a large, complex system. Although this approach limits the “freedom” of syntactic expression, it helps us steer our effort to develop an innovative and efficient hardware architecture.

After discussing the fundamentals in Part I, the book illustrates more complicated and sophisticated designs in the SoC context. Along the way, readers will learn many system-level concepts, including the derivation of a soft-core processor and IP (intellectual property) core based system, the partition and integration of software and hardware, and the development of custom I/O peripherals and hardware accelerators.

Although the book is intended for beginning designers, the examples follow strict design guidelines and prepare readers for future endeavors. The coding and design practice is “forward compatible,” by which we mean the following:

- The same practice can be applied to large designs in the future.
- The same practice can aid other system development tasks, including simulation, timing analysis, verification, and testing.
- The same practice can be applied to ASIC technology and different types of FPGA devices.
- The code can be accepted by synthesis software from different vendors.

**Audience and prerequisites**  The intended audience is students in an advanced digital design course as well as practicing engineers who wish to learn FPGA- and HDL-based developments. Readers need to have a basic knowledge of digital systems, usually a required course in electrical engineering and computer engineering curricula, and a working knowledge of the C/C++ language. Prior exposure to computer architecture, embedded system, and operating system is not necessary but will be helpful.

**Changes for the MicroBlaze MCS SoC Edition**

This book is the successor edition of *FPGA Prototyping by Verilog Examples: Xilinx Spartan 3 Version*. The *System Verilog* in the title reflects the fact that the book uses the new language constructs of SystemVerilog. The most significant change is that the new edition presents the hardware in the SoC context and covers many system-level concepts. Instead of treating each module as an isolated entity, the book integrates them into a single coherent SoC platform that allows readers to explore both hardware and software “programmability” and develop complex and interesting embedded system projects. The major revisions in this edition are the following:

- Add four general-purpose peripheral modules: multi-channel PWM (pulse width modulation), I²C controller, SPI controller, and XADC (Xilinx analog-to-digital converter) controller.
- Introduce a music synthesizer constructed with a DDFS (direct digital frequency synthesis) module and an ADSR (attack-decay-sustain-release) envelope generator.
- Expand the original video controller into a complete stream-based video subsystem that incorporates a video synchronization circuit, a test-pattern gen-
erator, an OSD (on-screen-display) controller, a sprite generator, and a frame buffer.

- Expand the coverage of timing model and provide an in-depth discussion of blocking and nonblocking statements.
- Introduce basic concepts of software-hardware co-design with Xilinx MicroBlaze MCS soft-core processor.
- Provide an overview of the bus interconnect and interface circuit.
- Introduce basic embedded system software development.
- Suggest additional modules and peripherals for interesting and challenging projects.

Logistics

FPGA prototyping board  This book is prepared to be used with the Nexys 4 DDR FPGA prototyping board manufactured by Digilent Inc. It contains an Artix FPGA device and the needed I/O peripherals. All HDL codes and discussions of this book can be applied to this board directly. The less expensive Basys 3 board can be used as well. This board incorporates fewer I/O peripherals and contains a smaller FPGA device.

Most peripherals discussed in the book are de facto industrial standards and the corresponding HDL codes can be used for other FPGA boards as long as they provide adequate analog interface circuits and connectors. Another option is to use stand-alone I/O peripheral modules or to construct the circuits on a breadboard.

Software  The book uses the Xilinx Vivado WebPack edition for hardware development and Xilinx SDK for software development. Both software packages are free and can be downloaded from Xilinx’s website.

PC accessories  The design examples involve interfaces to several PC peripheral devices, including a USB keyboard, a USB mouse, a VGA compatible monitor, and a powered speaker. These accessories are widely available and probably can be obtained from an old PC.

Book organization

The book is divided into four major parts. Part I introduces the elementary HDL constructs and their hardware counterparts, and demonstrates the construction of a basic digital circuit with these constructs. It consists of six chapters:

- Chapter 1 describes the skeleton of an HDL program, the basic language syntax, and the logical operators. Gate-level combinational circuits are derived with these language constructs.
- Chapter 2 provides an overview of an FPGA device, prototyping board, and development flow.
- Chapter 3 introduces HDL’s relational and arithmetic operators and routing constructs. These correspond to medium-sized components, such as comparators, adders, and multiplexers. Module-level combinational circuits are derived with these language constructs.
• Chapter 4 presents the codes for memory elements and the construction of “regular” sequential circuits, such as counters and shift registers, in which the state transitions exhibit a regular pattern.

• Chapter 5 discusses the construction of a finite state machine (FSM), which is a sequential circuit whose state transitions do not exhibit a simple, regular pattern.

• Chapter 6 presents the construction of an FSM with data path (FSMD). The FSMD is used to implement the register-transfer (RT) methodology, in which the system operation is described by data transfers and manipulations among registers.

• Chapter 7 covers the methods to infer FPGA’s internal memory modules, which can then be used to construct buffers and lookup tables.

• Chapter 8 provides an in-depth coverage of the timing model and data types and discusses an alternate coding style. This chapter can be skipped without affecting the remaining chapters.

Part II introduces the hardware construction of an FPro system and the development of embedded software. A basic “vanilla” FPro system, which contains a timer core, a UART (universal asynchronous receiver and transmitter) core, a GPI (general-purpose input) core, and a GPO (general-purpose output) core, is used to illustrate the key concepts of the process. It consists of four chapters:

• Chapter 9 introduces the SoC development and provides an overview of the hardware organization and software structure of the FPro platform.

• Chapter 10 discusses the software development for an embedded system and the basic coding techniques to access low-level I/O cores.

• Chapter 11 covers the FPro bus protocol and the bus interface circuit and demonstrates the construction of basic GPI, GPO, and timer cores.

• Chapter 12 presents the construction of a more sophisticated UART core and the derivation of software device drivers.

Part III applies the techniques from Parts I and II to develop an array of I/O cores for the peripherals on the Nexys 4 DDR prototyping board. The I/O cores are constructed from scratch with custom hardware and device driver. Part III consists of nine chapters:

• Chapter 13 discusses the Xilinx device’s internal analog-to-digital converter (XADC) and derives an interface circuit to retrieve the analog readings.

• Chapter 14 presents the design of a multi-channel PWM core and demonstrates its application for LED brightness adjustment and servo motor control.

• Chapter 15 converts the seven-segment LED control circuit and the switch debouncing circuit of Part I into I/O cores and integrates them into an FPro system.

• Chapter 16 provides an overview of the SPI protocol, covers the design of an SPI controller core, and shows its operation with Nexys 4 DDR board’s ADXL362 three-axis accelerometer.

• Chapter 17 provides an overview of the I^2C protocol, discusses the design of an I^2C controller core, and demonstrates its operation with Nexys 4 DDR board’s ADT7420 temperature sensor.

• Chapter 18 covers the design of a PS2 controller core, which can be connected to a PS2 mouse or a PS2 keyboard, and discusses the device driver routines
to read and decode keyboard scan codes and to obtain and process mouse movement information and button activities.

- Chapter 19 discusses the construction of a DDFS (direct digital frequency synthesis) controller core with amplitude and frequency modulation and demonstrates its application as a music synthesizer.
- Chapter 20 augments the music synthesizer with an ADSR (attack-decay-sustain-release) envelope generator core, which can produce sound mimicking various music instruments.

Part IV discusses the development of a stream-based video subsystem. The subsystem provides a framework to generate and mix multiple video sources into a single video data stream for display. It consists of four chapters:

- Chapter 21 introduces the concept of stream data processing and constructs a basic video system with a test-pattern generator, a color-to-grayscale conversion circuit, and a frame synchronization circuit.
- Chapter 22 provides an overview of the FPro video subsystem framework and the FPro video core structure and demonstrates the stream interface with a line buffer.
- Chapter 23 presents the design of a sprite circuit, which adds an overlay of small animated objects on the screen, and applies the technique for a mouse pointer core and a “Pac-Man ghost character” core.
- Chapter 24 discusses the design of an OSD (on-screen-display) controller core, which produces an overlay of text similar to the subtitles on a TV screen.
- Chapter 25 covers the design of a frame buffer, which maintains a bitmap for one screen.

In addition to the main text chapters, the book includes an Appendix with four tutorials. The tutorials consist of the following:

- Develop, synthesize, and implement a digital circuit on the Nexys 4 DDR board with Vivado.
- Perform simulation of an HDL program with Vivado’s built-in simulator.
- Configure and instantiate Xilinx IP cores.
- Construct a basic FPro system with a Xilinx microBlaze MCS IP core and develop software with the Xilinx SDK platform.

**Companion Website**

On an accompanying website (http://academic.csuohio.edu/chn.p) additional information is available, including the following materials:

- Errata
- HDL and C/C++ code listings and relevant files
- Links to synthesis and simulation software
- Links to reference materials

The printed book contains a number of color figures. They are shown as grayscale in the printed version. These figures can be found in full color on the website as well.
Errata  The book is self-prepared, which means that the author has produced all aspects of the text, including illustrations, tables, code listings, indexing, and formatting. As errors are always bound to happen, the accompanying website provides an updated errata sheet and a place to report errors.

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